a first intermediate layer having a first thickness and provided above the semiconductor substrate; and

a second intermediate layer having a second thickness thinner than the first thickness and provided above the first intermediate layer.

19. (New) A semiconductor device according to claim 18, further comprising:

a lowermost layer nearest to the semiconductor substrate and provided below the first intermediate layer; and

an uppermost layer farthest from the semiconductor substrate and provided above the second intermediate layer.

20. (New) A semiconductor device according to claim 19, wherein a wiring pitch of the first intermediate layer is greater than that of the second intermediate layer.

21. (New) A semiconductor device according to claim 19, wherein the first intermediate layer is a layer on which a power source line is formed.

22. (New) A semiconductor device according to claim 19, wherein the first intermediate layer comprises a first area having signal lines and a second area having power source lines, and a pitch of the power source lines is greater than that of the signal lines.

23. (New) A semiconductor device according to claim 19, wherein the first intermediate layer comprises a first area having signal lines and a second area having power source lines, and a width of each of the power sources lines is greater than that of the signal lines.

24. (New) A semiconductor device according to claim 19, wherein the first intermediate layer is substantially as thick as the uppermost layer.

25. (New) A semiconductor device according to claim 19, wherein the second intermediate layer is substantially as thick as the lowermost layer.

26. (New) A semiconductor device according to claim 19, wherein all of the uppermost layer, the lowermost layer and the first and second intermediate layers are metal layers.

27. (New) A semiconductor device comprising:

a semiconductor substrate;

an IP core area on the semiconductor substrate;

a peripheral area on the semiconductor substrate except for the IP core area;

a first intermediate layer having a first thickness and provided above the semiconductor substrate in the IP core area; and

a second intermediate layer having a second thickness smaller than the first thickness and provided above the first intermediate layer in the IP core area.

28. (New) A semiconductor device according to claim 27, further comprising:

a lowermost layer nearest to the semiconductor substrate and provided below the first intermediate layer; and

an uppermost layer farthest from the semiconductor substrate and provided above the second intermediate layer.

29. (New) A semiconductor device according to claim 28, wherein the first intermediate layer is a layer on which a core power source line is formed.

30. (New) A semiconductor device according to claim 28, wherein a wiring pitch of the first intermediate layer is greater than that of the second intermediate layer.

31. (New) A semiconductor device according to claim 28, wherein the first intermediate layer is substantially as thick as the uppermost layer.

32. (New) A semiconductor device according to claim 28, wherein the second intermediate layer is substantially as thick as the lowermost layer.

33. (New) A semiconductor device according to claim 28, wherein the first intermediate layer comprises a first area having signal lines and a second area having power source lines, and a pitch of the power source lines is greater than that of the signal lines.

34. (New) A semiconductor device according to claim 28, wherein the first intermediate layer comprises a first area having signal lines and a second area having power source lines, and a width of each of the power source lines is greater than that of the signal lines.

35. (New) A semiconductor device according to claim 28, wherein all of the uppermost layer, the lowermost layer and the first and second intermediate layers are metal layers.